WHAT IS CLAIMED IS;

1. A method for the formation of rectifying junctions on alloy-semiconductors comprising the steps of:

photo-electrochemical removal of one component of the alloy material and

chemical etching of another component of the alloy

to produce a positive-intermediate-negative (PIN) structure semiconductor.

2. The method according to Claim 1, wherein the alloy semiconductor comprises a combination of Group II element and a Group VI element.

3. The method according to Claim 2, wherein the alloy semiconductor comprises CdTe.

4. The method according to Claim 2, wherein the alloy semiconductor comprises CdZnTe.

5. The method according to Claim 2, wherein the alloy semiconductor comprises HgZnCdTe.

6. The method according to Claim 2, wherein the alloy semiconductor comprises HgCdZnSe.

7. A method for the formation of rectifying junctions on alloy-semiconductors comprising the steps of:

photo-electrochemical removal of one component of the alloy material to produce one portion of the junction and

deposition of a second component to produce a second portion of the junction

to produce a positive-intermediate-negative (PIN) structure semiconductor.

8. The method according to Claim 7, wherein the alloy semiconductor comprises a combination of Group II element and a Group VI element.

9. The method according to Claim 8, wherein the alloy semiconductor comprises CdTe.

10. The method according to Claim 8, wherein the alloy semiconductor comprises CdZnTe.

11. The method according to Claim 8, wherein the alloy semiconductor comprises HgZnCdTe.

12. The method according to Claim 8, wherein the alloy semiconductor comprises HgCdZnSe.

13. A positive-intermediate-negative (PIN) structure semiconductor constructed by the process consisting of the steps of:

photo-electrochemical removal of one component of the alloy material and

chemical etching of another component of the alloy

to produce the positive-intermediate-negative (PIN) structure semiconductor.

14. The PIN structure semiconductor according to Claim 13, wherein the alloy semiconductor comprises a combination of Group II element and a Group VI element.

15. The PIN structure semiconductor according to Claim 14, wherein the alloy semiconductor comprises CdTe.

16. The PIN structure semiconductor according to Claim 14, wherein the alloy semiconductor comprises CdZnTe.

17. The PIN structure semiconductor according to Claim 14, wherein the alloy semiconductor comprises HgZnCdTe.

18. The PIN structure semiconductor according to Claim 14, wherein the alloy semiconductor comprises HgCdZnSe.

19. A device for detecting and measuring an electrical response due to a single charge carrier in a room-temperature semiconductor, the device comprising:

a PIN structure semiconductor , said semiconductor having first and second ends;

a first electrode in electrical contact with said first end, said first electrode biased at a first electrical potential;

a second electrode in electrical contact with said second end, said second electrode biased at a second electrical potential, said first potential greater than said second potential;

wherein the PIN structure semiconductor is constructed by the process consisting of the steps of:

photo-electrochemical removal of one component of the alloy material and

chemical etching of another component of the alloy

to produce the PIN structure semiconductor.

20. The device according to Claim 19, wherein the alloy semiconductor comprises a combination of Group II element and a Group VI element.

21. The device according to Claim 20, wherein the alloy semiconductor comprises CdTe.

22. The device according to Claim 20, wherein the alloy semiconductor comprises CdZnTe.

23. The device according to Claim 20, wherein the alloy semiconductor comprises HgZnCdTe.

24. The device according to Claim 20, wherein the alloy semiconductor comprises HgCdZnSe.